VIA TELEFAX 703-308-7722 TO EXAMINER HOANG

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Atty. Docket No. 8040-1041

PATENTS

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

(W.C.) 15/Response G. Study 6-12-03

In re application of

Masamoto TAGO et al. Confirmation No. 9072

Serial No. 09/613,331 GROUP 2818

Filed July 7, 2000 Examiner Quoc Dinh Hoang

SYSTEM SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

RESPONSE AFTER FINAL REJECTION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This responds to the Official Action of February 6, 2003.

This application is believed to be in condition for allowance at the time of the next Official Action.

As a procedural matter, applicants note that Form PTO-892 issued as an attachment to the Official Action of February 6,

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Certificate of Transmission

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office on June 4, 2003.

Linda Sayyad

Linda Sayyad

2003, to which the present filing responds, identifies the newly-cited WATANABE et al. reference correctly by inventor name, but it identifies the patent number as "278148" instead of "6278148". Applicants therefore respectfully request that the next Official Action include a corrected Form PTO-892.

The Official Action rejects the claims under 35 USC §102(b) as being anticipated by SAITOU et al. 5,162,240. Reconsideration and withdrawal of this rejection are respectfully requested for the following reasons:

The Official Action rejects claims 1, 2, 6, 7, and 9-24 under 35 USC §103(a) as being unpatentable over SAITOU et al. in view of WATANABE et al. Reconsideration and withdrawal of this rejection are respectfully requested for the following reasons:

In connection with the rejected method claims, the Official Action asserts that the SAITOU et al. reference teaches or suggests all of the recited method steps. The Official Action acknowledges, however, that SAITOU et al. do not clearly disclose the requirement that each of the functional blocks comprises a plurality of gates. It is this feature for which the secondary WATANABE et al. reference is offered.

Applicants note that independent method claim 12 includes the following steps:

> a) fabricating a system LSI cell portion ...,
>
> b) fabricating a global wiring layer separate from the fabricated system LSI cell portion by forming a wiring layer on a semiconductor substrate, and

c) laminating the system LSI cell portion with the separately fabricated global wiring layer such that electrical interconnection among said gates disposed in separate said functional blocks are electrically connected to each other by the global wiring layer.--

One of the features of method step b) is that the recited fabrication of the global wiring layer be separate from the fabricated system LSI cell portion. This characteristic underlies step c), which recites the lamination of the system LSI cell portion fabricated in step a) with the global wiring layer separately fabricated in step b). Applicants respectfully suggest that these characteristics of the recited method are neither taught nor suggested by either of the applied references.

All of the above-identified characteristics are attributed by the Official Action to the SAITOU et al. reference. The embodiment 1 of SAITOU et al. is described beginning in the middle of column 6 and continuing to the middle of column 11. In connection with this and the other embodiments described in the reference, the Official Action identifies a recited global wiring layer element 20 of SAITOU et al. Applicants note that the reference identified as element 10, which underlies the thin film circuit 20, as a thick film wiring substrate. The description of the fabrication of the thick film wiring substrate 10 concludes on column 8, line 33.

Significantly, beginning on the following line, the description of the fabrication method continues by reference to "the thin film circuit 20 formed thereon". (Emphasis added). As

is evident from this passage, the thin film circuit 20 is formed in place, on the thick film wiring substrate 10. In stark contrast to the present invention as disclosed and as recited in the various independent method claims, the system LSI cell portion and the global wiring layer are not separately formed and, after their respective formation, laminated together in a final step.

The subsequent embodiments described in the SAITOU et al. reference modify various details of the structure and method described therein, but no variation exists in connection with the formation of the thin film circuit 20. This is further supported by the description beginning in column 13, line 63 in connection with embodiment 5, where SAITOU et al. state:

> The thin film circuit substrate of FIG. 1 formed on the connecting conductor pad is formed using polyimide resin as the insulation layer 21 and copper as the conductor 22 by means of the conventional thin film technique. Thus, the thick and thin film hybrid multilayer wiring substrate is formed. (Emphasis added)

As is clearly recited in this passage, the feature that the Official Action characterizes as being global wiring layer is not separately formed and then laminated with the system LSI cell portion, but is instead formed directly on the first layer.

Again, in column 16 in connection with embodiment 9, SAITOU et al. state beginning on line 50:

> In the foregoing description, the modification is made on the basis of the result of the defect inspection for the thick film wiring substrate 10, while the inspection of disconnection and short circuit is performed before the LSI is connected finally, that is, after the thin film wiring substrate

20 is formed on the thick film wiring substrate 10. (Emphasis added).

Similar to independent method claim 12 as excerpted above, independent method claim 16 also includes a step of fabricating a system LSI cell portion, the separate step of fabricating a global wiring layer, and a third step of laminating the system LSI cell portion with the global wiring layer, as does independent method claim 17.

In connection with independent apparatus claims 1, 6, and 24, each recites a global wiring layer which has a wiring layer on a semiconductor substrate and which is laminated with the system LSI cell portion such that the functional blocks are electrically connected to each other. Such feature is neither taught nor suggested by SAITOU et al., considering either the narrative description of the device disclosed thereby or the illustration in the drawing figures thereof. The thin film 20 includes no element that can reasonably be construed as a semiconductor substrate.

Furthermore, the secondary WATANABE et al. reference does not overcome the shortcomings of SAITOU et al. Figure 4 of WATANABE et al. is representative of the apparatus disclosed thereby, considered from a logical block level. As illustrated in such drawing, two separate logical blocks are arranged with a dynamic memory intervening. A sixth wiring layer WR1 operates as an electrical interconnection between the respective logical blocks.

However, such sixth wiring layer, while it may serve to provide electrical interconnection between gates of different functional blocks, clearly fails to meet the requirements that it be "a wiring layer on a semiconductor substrate [that] is laminated with the system LSI cell portion".

Accordingly, neither the primary SAITOU et al. reference nor the secondary WATANABE et al. reference provides teaching or suggestion of the characteristics attributed to the global wiring layer recited in either the method or apparatus independent claims.

In light of the amendments described above and the arguments offered in support thereof, applicants believe that the present application is in condition for allowance and an early indication of the same is respectfully requested.

If the Examiner has any questions or requires further clarification of any of the above points, the Examiner may contact the undersigned attorney so that this application may continue to be expeditiously advanced.

Respectfully submitted,

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